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2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/751,841	HEITKAMP ET AL.
	Examiner	Art Unit
	Khanh Dang	2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 21, 22, and 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 21 and 22, the essential structural cooperative relationships between elements recited in claim have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2171.02.

With regard to claim 26, the essential structural cooperative relationships between the means plus functions recited in claim have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2171.02.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-9, 11-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Khosrowpour et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims do not define any structure that differs from Khosrowpour et al. With regard to claims 1, 5, 6, 7, 8, 11, 12, 13, 14, 15, and 26, Khosrowpour et al. discloses a control system, comprising: a bus (104); a master device (102) connected to the bus and configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the bus during the address interval, and transmit or receive a command or data during the data interval; and a plurality of slave devices connected to the bus and configured to detect commencement of the bus cycle, sample the destination address from the bus a predetermined amount of time after commencement of the address interval, and transmit or receive a command or data during the data interval. Note that SMB (104) employs I2C Bus. I2C is a 2-wire serial interface standard defined by Philips Semiconductor. The I2C Bus physically consists of 2 active wires and a ground connection. The active wires, SDA and SCL, are both bi-directional. SDA is the Serial Data line and SCL is the Serial Clock line. The I2C interface is a master/slave type interface. Only two lines (clock and data) are required for full duplexed communication between multiple devices. With I2C, each IC on the bus has a unique address. A device that controls signal transfers on the line in addition to controlling the clock

frequency is the master and a device that is controlled by the master is the slave. The master can transmit or receive signals to or from a slave, respectively, or control signal transfers between two slaves, where one is the transmitter and the other is the receiver. I2C bus support more than one master connected to one bus. It is possible to combine several masters, in addition to several slaves, onto an I²C-bus to form a multi-master system. To begin communication, the bus master places the address of the device with which it intends to communicate (the slave) on the bus. All ICs monitor the bus to determine if the master device is sending their address. Only the device with the correct address communicates with the master. I2C Specification is readily available at Philips Semiconductor. Also see at least claim 1; Figs. 1, 1A, and 2 and description thereof). With regard to claim 3, see above and Fig. 1A and description thereof. With regard to claim 9, the sample circuit of Khosrowpour et al. resamples data bit after the resetof the control logic after a predetermined time. With regard to claim 16, since the system of Khosrowpour et al. is a server-type and can be controlled remotely it can be said that such a system is a "network device." With regard to claims 17 and 18, one using the system of Khosrowpour et al. would have performed the same steps set forth in claims 17 and 18.

Claims 1, 2, 5-9, 11-18, 23, 24, 26-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Dickson et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims, after the word "comprising," do not define any structure that differs from Dickson et al. With regard to claims 1-3, 5-9, 11-16, 23, 24, 26-29, Dickson et al. discloses a network device, comprising: a plurality of redundant buses (17, 20); a plurality of redundant master controllers (18, 19) connected to corresponding ones of the buses (bus shown in Fig. 1 for providing connection between 17 and 24 via 18, not labeled, perpendicular to bus 20, bus 20), one of the master controllers being an active master and other ones of the master controllers being standby masters, the active master being configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the corresponding bus during the address interval, and transmit or receive a command or data during the data interval; and a plurality of slave controllers (peripheral device controllers, see also col. 2, lines 34-37) connected to the bus and configured to detect commencement of the bus cycle, sample the destination address from the bus a predetermined amount of time after commencement of the address interval, and transmit or receive a command or data during the data interval. See at least Figs. 1-4 and description thereof. With regard to claims 17 and 18, one using the system of Dickson et al. would have performed the same steps set forth in claims 17 and 18.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour et al.

Khosrowpour et al., as discussed above, disclsose the claimed invention except the use of a "5 clock cycles." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use "5 clock cycle" in Khosrowpour et al., since using a particular number of cycles is an obvious design choice; and only involves routine skill in the art. In any event, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dickson et al.

Dickson et al., as discussed above, discloses the claimed invention except the use of master controllers as "router" and slave controllers as "switching and forwarding modules." It would have been obvious to one of ordinary skill in the art at the time the

invention was made to use the system of Dickson et al. in a network environment (note that every network includes routers and switches), since it has been held that the manner in which a claimed apparatus is intended to be employed (in a network environment) does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicant's arguments filed 10/09/2003 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Yamamoto*, 740 F2.d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification can not be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claimed language will not be warranted.

The 112, 2nd paragraph rejection:

With regard to claim 26, Applicants argued that the "system also include several means-plus-function elements that perform an operation 'on the bus.'" In response, the Examiner maintains the 112 rejection of claim 26. Claim 26 is an apparatus claim claiming a plurality of different means. However, the essential structural cooperative relationships between these "means" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2171.02.

The Khosrowpour et al. 102 reference:

With regard to claim 1, Applicants argued that Khosrowpour et al. "does not disclose a bus cycle that includes an address interval and a data interval." Contrary to Applicants' argument, it is clear even by Applicants' own admission that Khosrowpour et al., col. 2, lines 11-23, that "the master transmits several data bits implementing a command, where each bit is combined with clocking pulses [defining the so-called 'interval']" and "each command includes at least one command [data used to perform a desired function] bit and corresponding address bit" (col. 2, lines 32-34). The initial command bit is different from the command bit which is used to perform a desired function. This is in agreement with the Examiner's explanation (Office Action, page 2) regarding i2C bus and I2C specification. The fact that since the bus of Khosrowpour et al.'s bus is I2C bus, it must strictly adhere to the I2C specification. Further, contrary to

Applicants' argument, the Examiner explanation (Office Action, page 2) regarding I2C bus and I2C specification is fact, not allegation. Applicants are, again, reminded that I2C specification is readily available from Philips Semiconductor (through the Internet, for example). Applicants also argued that "nothing in these figures [1, 1A, 2], or description thereof, supports the Examiner's allegations." Contrary to Applicants' argument, Figures 1, 1A, and description thereof clearly disclose a master or a plurality of master communicating with a plurality of slaves using I2C bus (which must strictly adhere to the specification of I2C). Applicants further argued that Khosrowpour et al. "does not disclose or suggest a plurality of slave devices that, among other things, begin to sample a destination address from the bus one or more clock cycle after commencement of the address interval." Contrary to Applicants' argument, it clear that at least the pulse detection circuit and command decode circuit of at least one slave detects the command pulses and retrieves and decodes the command (each command includes at least one command [data used to performed a desired function] bit and corresponding address bit) after at least one clock cycle. See at least col. 2, lines 2-4). It is also true for any I2C bus that all ICs monitor the bus to determine if the master device is sending their address. Only the device with the correct address communicates with the master. I2C Specification is readily available at Philips Semiconductor. With regard to claim 3, Applicants argued that Khosrowpour et al. does not disclose "a data/address interval signal line." Contrary to Applicants' argument, it is first noted the fact that since the bus of Khosrowpour et al.'s bus is I2C bus, it must strictly adhere to the I2C specification. The data line of the I2C (Fig. 1 A) is used to transmit several data bits

implementing a command, where each bit is combined with clocking pulses [defining the so-called 'interval']" and "each command includes at least one command [data used to performed a desired function] bit and corresponding address bit" (col. 2, lines 32-34). With regard to claim 13, Applicants argued that Khosrowpour et al. does not and the Examiner did not address the features of claim 13. Contrary to Applicants' argument, the Examiner provides clear explanation (Office Action, page 2) regarding I2C bus and I2C specification. Reference to Figures 1, 1a, 2, and description thereof were also given to Applicants. It is clear from at least Fig. 1a that the M_PRESENT signal line (used for all communication purposes) performs the claimed function set forth in claim 13. With regard to claim 17, Applicants argued that Khosrowpour et al. does not disclose "an address interval followed by a data interval." In response, it is clear from Khorowpour et al. that the address interval is followed by a data interval. Applicants appear to confuse the "initial command bit" with the "command bit" which follows the address bit. See at least col. 11, lines 5-12. See also explanation regarding claim 1 and previous Office Action (page 2).

The Khosrowpour et al. 103 rejection:

With regard to Applicants' argument regarding to the 103 rejection of claim 10, it is the Examiner's position that selecting a particular number of clock cycles is only a matter of design choice, and involves only routine skill in the art. In any event, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

The Dickson et al. 102 rejection:

With regard to claim 1, Applicants argued that Dickson et al. does not disclose that "a slave begins to sample a destination address from a bus one or more clock cycle after commencement of an address interval." Contrary to Applicants' argument, it is inherent that the slave must "sample" the bus via SBS 17 in order to know whether its address is selected and begins to enable its transmit buffer and responds. Applicants' argument regarding claim 2 is moot in view of a change from the Examiner's position re buses. See above. The rejection of claim 3 over Dickson et al. is hereby withdrawn in view of Applicants' argument. With regard to claims 17 and 26, it is clear that it is inherent that the slave must "sample" the bus via SBS 17 in order to know whether its address is selected and begins to enable its transmit buffer and responds. With regard to claim 27, Applicants' argument regarding claim 27 is moot in view of a change from the Examiner's position re buses. See above.

The Dickson et al. 103 rejection:

Applicants did not separately argued the 103 rejection over Dickson et al.

Allowable Subject Matter

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21 and 22 are allowable.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner